IN THE SPECIFICATION:

Please amend the following paragraph starting on page 29, line 2 as follows:

The stored data selecting section 17 has the same configuration as the counterpart 17 of the first embodiment. Specifically, the byte selection controller 18 receives the selected correction address signal SSCAD and a logical sum SSCO, output by gate 34, of the correspondence detection signals SCO1 and SC02 and generates the byte selection control signals SSa through SSd in accordance with the same logic as that applied to the first embodiment. The byte selector 19 receives the ROM data signal SROM with a width of 4 bytes and the rotated data SRT output from the data rotator 33. In response to the byte selection control signals SSa through SSd, the byte selector 19 selects, on a byte-by-byte basis, either the ROM data signal SROM or the rotated data SRT and then outputs a selected combination of bytes as a data signal SDT to the microprocessor 12.